Notice of Allowability	Application No.	Applicant(s)	
	10/815,015	SLAWECKI, DARREN	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendments filed on 01/25/2006*.

2. ☒ The allowed claim(s) is/are *1-37*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Response to Amendment

1. The amendment received on 01/25/2006 has been reviewed and considered with the following results:

As to the prior art rejections to claims 14-18, 21, and 33; in view of Applicant's amendments and arguments with respect to the previous prior art rejections mailed on 12/13/2005, Applicant's arguments have been considered, and found persuasive, as such; the prior art rejections have been withdrawn. Therefore the case is found to be in allowance condition for the reasons as set for below.

REASON FOR ALLOWANCE

2. The following is an examiner's statement of reasons for allowance:

Applicant has amended the base claims to include the claims that would be allowable if rewritten in independent form as stated in the previous Office Action. As to pending claims of the application, the prior art of record fails to disclose or fairly suggest a delay circuit (500 in instant Fig. 5), as recited in claim 1, having specific structural limitation such as a falling edge delay circuit coupled to the pull up path to control delay of a falling edge of the reference signal, wherein the pull up path includes a first transistor to selectively couple the logic output to the falling edge delay circuit; and a rising edge delay circuit coupled to the pull down path to control delay of a rising edge of the reference signal, wherein the pull down path includes second and third transistors coupled in series to selectively couple the logic output to the rising edge delay

circuit, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a delay circuit (500 in instant Fig. 5), as recited in claim 11, having specific structural limitation such as an inverting enable circuit including a circuit input to receive a reference signal; a circuit output to output a delayed signal being a delayed inversion of the reference signal; a logic circuit including a logic input and a logic output; a first inverter coupling the circuit input to the logic input; a pull-up path coupled to the logic output; a pull down path coupled to the logic output; and a second inverter coupling the logic output to the circuit output; and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a circuit (500 in instant Fig. 5), as recited in claim 14, having specific structural limitation such as a NAND logic circuit (L1) having a first NAND input coupled to receive the reference clock signal (320), a second NAND input coupled to the enable input (325), and a NAND output; and an inverter circuit (L2) coupling the NAND output to the circuit output; a falling edge delay circuit (515, T2, T3) coupled to the enable circuit to control delay of a falling edge of the reference clock signal; and a rising edge delay circuit (510, T1) coupled to the enable circuit to control delay of a rising edge of the reference clock signal; and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest an integrated circuit (700 in instant Fig. 7), as recited in claim 22, comprising a clock distribution network to distribute a reference clock signal throughout the integrated circuit; and having specific structural limitation

such as each of clock delay circuits (500 in instant Fig. 5) comprising a clock enable circuit including a clock input to receive the reference clock signal; an enable input; a circuit output to output a delayed clock signal being a delayed response to the reference clock signal; a NAND logic circuit having a first NAND input coupled to receive the reference clock signal, a second NAND input coughed to the enable input and a NAND output; and an inverter circuit coupling the NAND output to the circuit output a falling edge delay circuit coupled to the enable circuit to control delay of a falling edge of the reference clock signal; and a rising edge delay circuit coupled to the enable circuit to control delay of a rising edge of the reference clock signal; latches each clocked according to the delayed clock signal output from each of the clock delay circuits; and logic clusters to compute logic values, the latches coupled to buffer the logic values between clock edges of the delayed clock signals; and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

5. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Busines1s Center (EBC) at 866-217-9197 (toll-free).

HLN
April 10, 2006

Terry D. Cunningham
Primary Examiner